REMARKS

Favorable reconsideration of this application is respectfully requested.

A new title is added as requested in the Office Action.

Claims 1-18 are present in this application, claims 12-18 being added by way of the present amendment. New claims 12-18 are clearly supported by the specification and thus no question of introduction no matter is believed to be added. Further, new claims 12-18 read on the elected species of Figures 1 and 2.

The present invention is directed to an image processing apparatus. The image processing apparatus has an image processing part which includes a buffer memory for data storage, and image processing unit which writes image data to the buffer memory, and a compression unit for compressing the image data read from the buffer memory. The buffer memory is connected to receive only the image data from the image processing unit. With such a configuration, the image processing apparatus can process data more efficiently by avoiding data transfers between the image processing part and an external memory.

Claims 1 and 2 stand rejected under 35 U.S.C. § 102(b) over U.S. 2001/001936 to Nakamura et al. Claims 3-11 are withdrawn from consideration.

Turning to the § 102 rejection, Nakamura et al. discloses in Figure 4 a block diagram of a digital camera 1. The main CPU 21 includes an image signal processor 211, JPEG section 212, and bus controller 218 all connected via bus 219. External memory 23 consisting of flash ROM 231 and DRAM 232 are connected via bus controller 218 to CPU 21. DRAM 232 is asserted to correspond to the buffer memory recited in claim 1.

DRAM 232 is "for accumulating image data or the like" (paragraph [0056], line 3). Bus controller 218 acts as a DMA controller allowing direct data transfer between each module for which a DMA channel is set up and the DRAM 232. As described in paragraphs [0069]-[0076], DMA channels are set up to allow direct data transfer between the DRAM and

the image signal processor, the JPEG section, the video encoder, and the memory card controller.

The buffer memory according to claim 1 is connected to receive only the image data from the image processing unit. Clearly, the DRAM 232 is connected to receive data from multiple elements and clearly does not suggest and teaches away from the image processing apparatus of claim 1. Accordingly, Claim 1 is believed to be patentably distinguishable over Nakamura et al.

New Claim 15 recites an image processing apparatus having first and second buffer memories connected in parallel for data storage, and image processing unit which alternatingly writes the image data into the first and second buffer memories, and a compressing unit for compressing the image data alternatingly read from the first and second buffer memories. Such a structure is clearly not disclosed or suggested by Nakamura et al.

It is respectfully submitted the present application is in condition for allowance, and the favorable decision to that effect is respectfully requested.

Respectfully submitted,

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